

BASIC MOTOR NEURON CIRCUIT

FIG. 1

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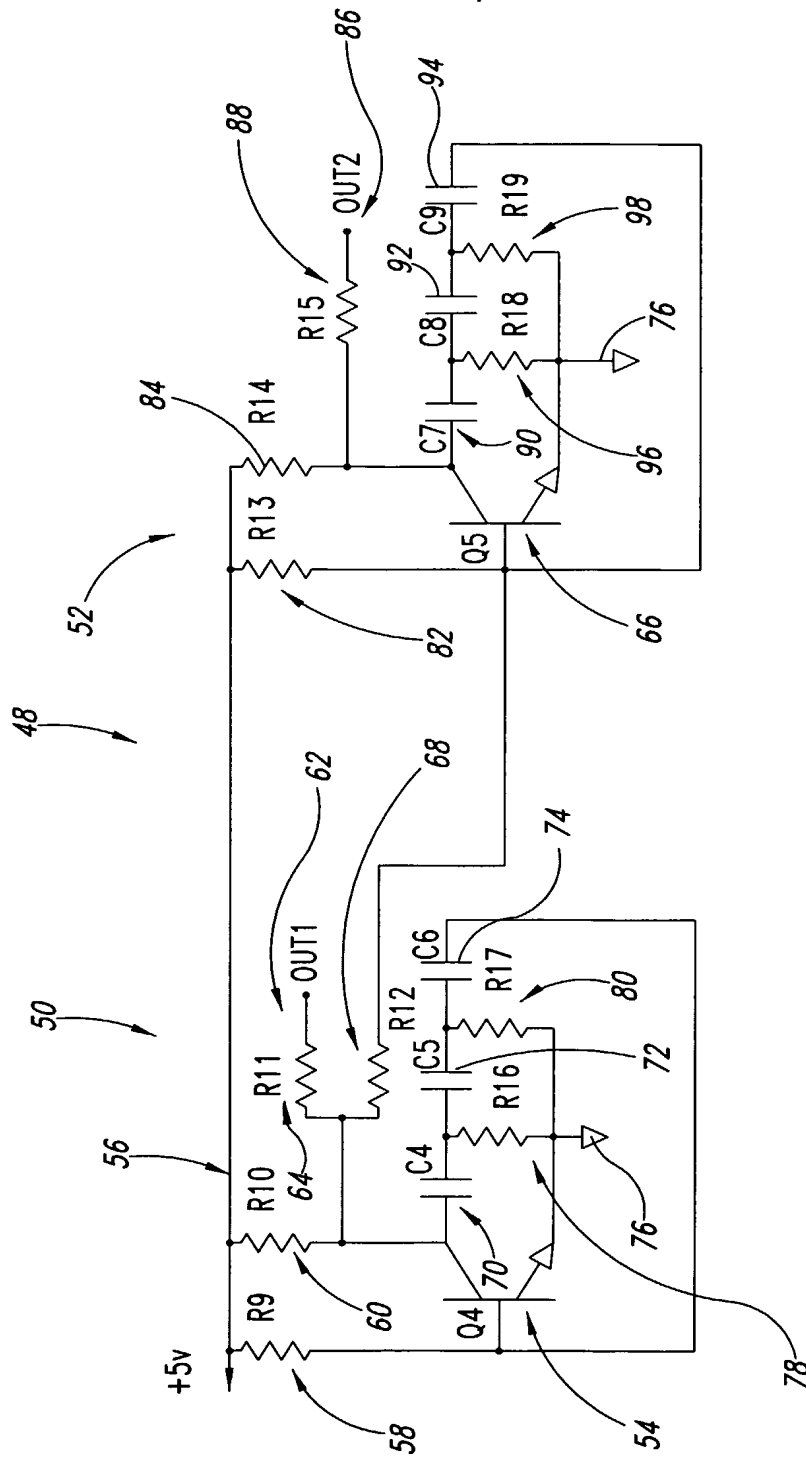


FIG. 2

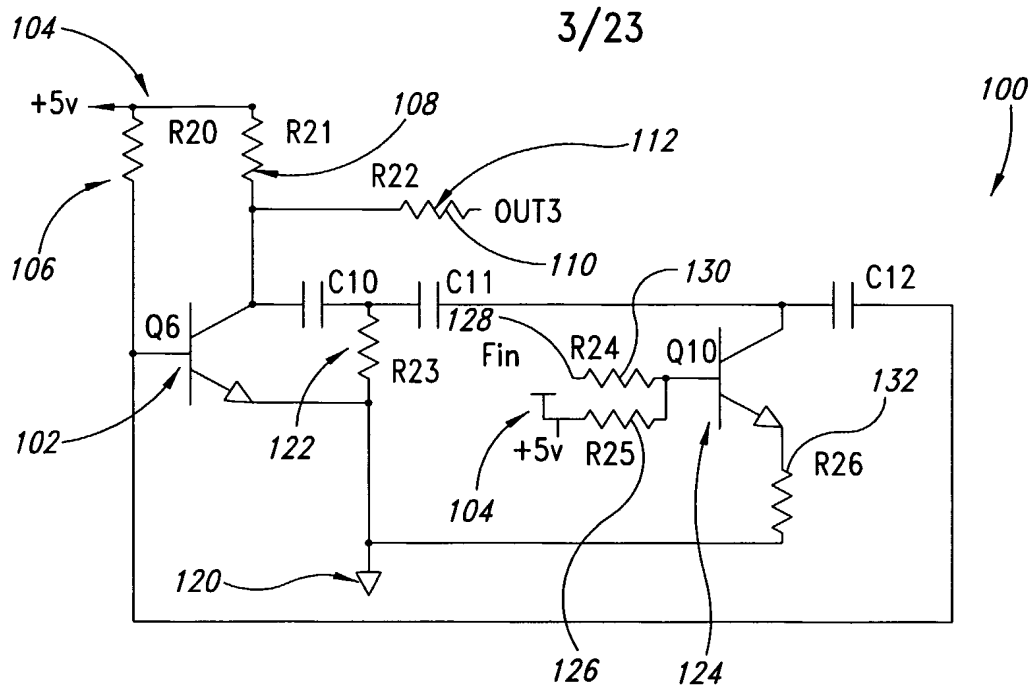


FIG. 3

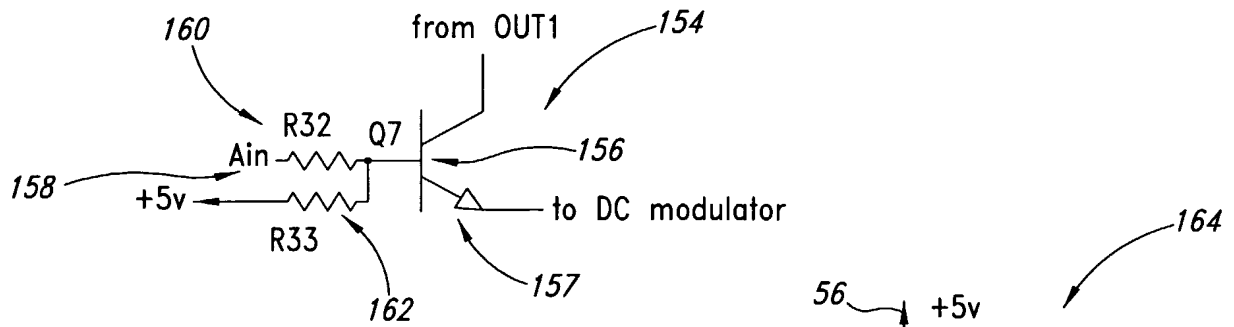


FIG. 5

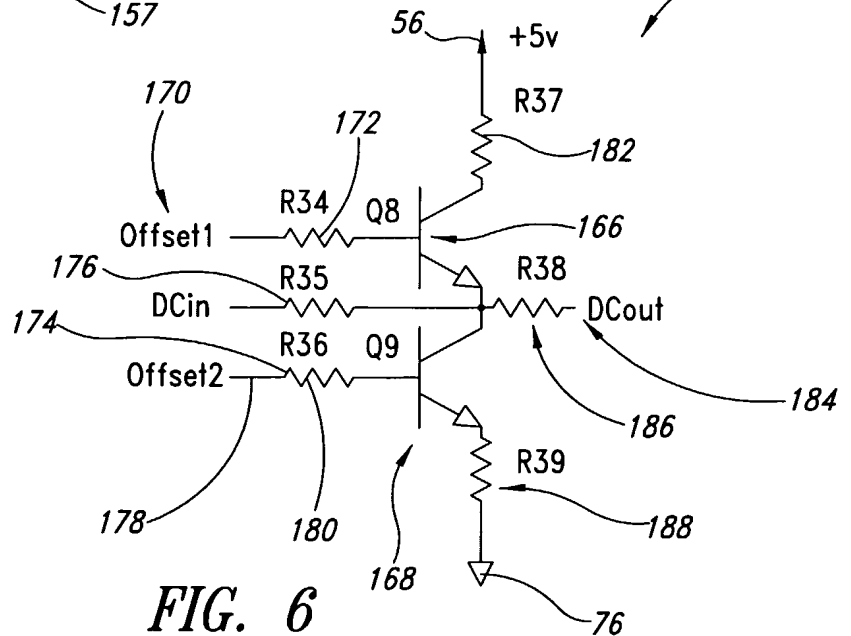


FIG. 6

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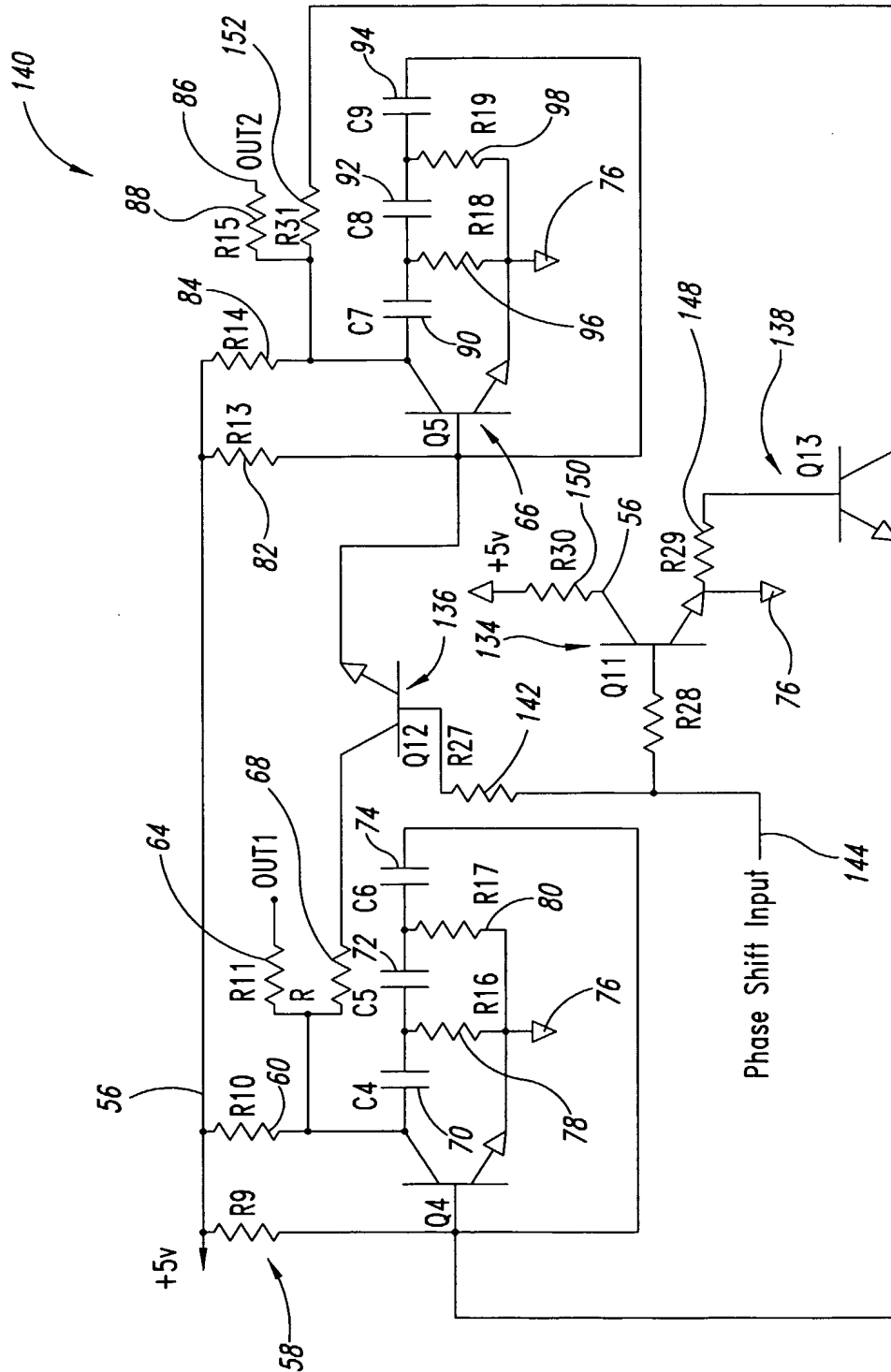


FIG. 4

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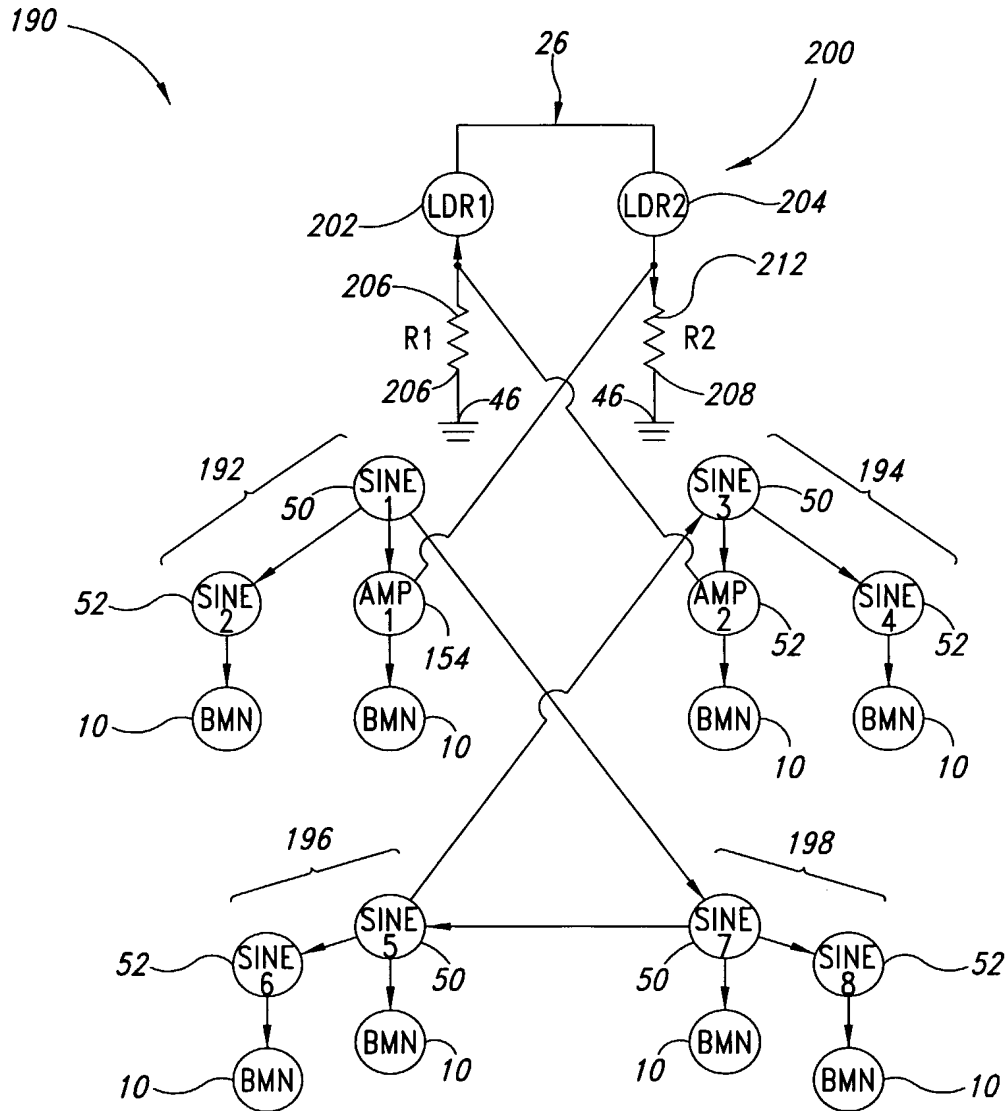


FIG. 7

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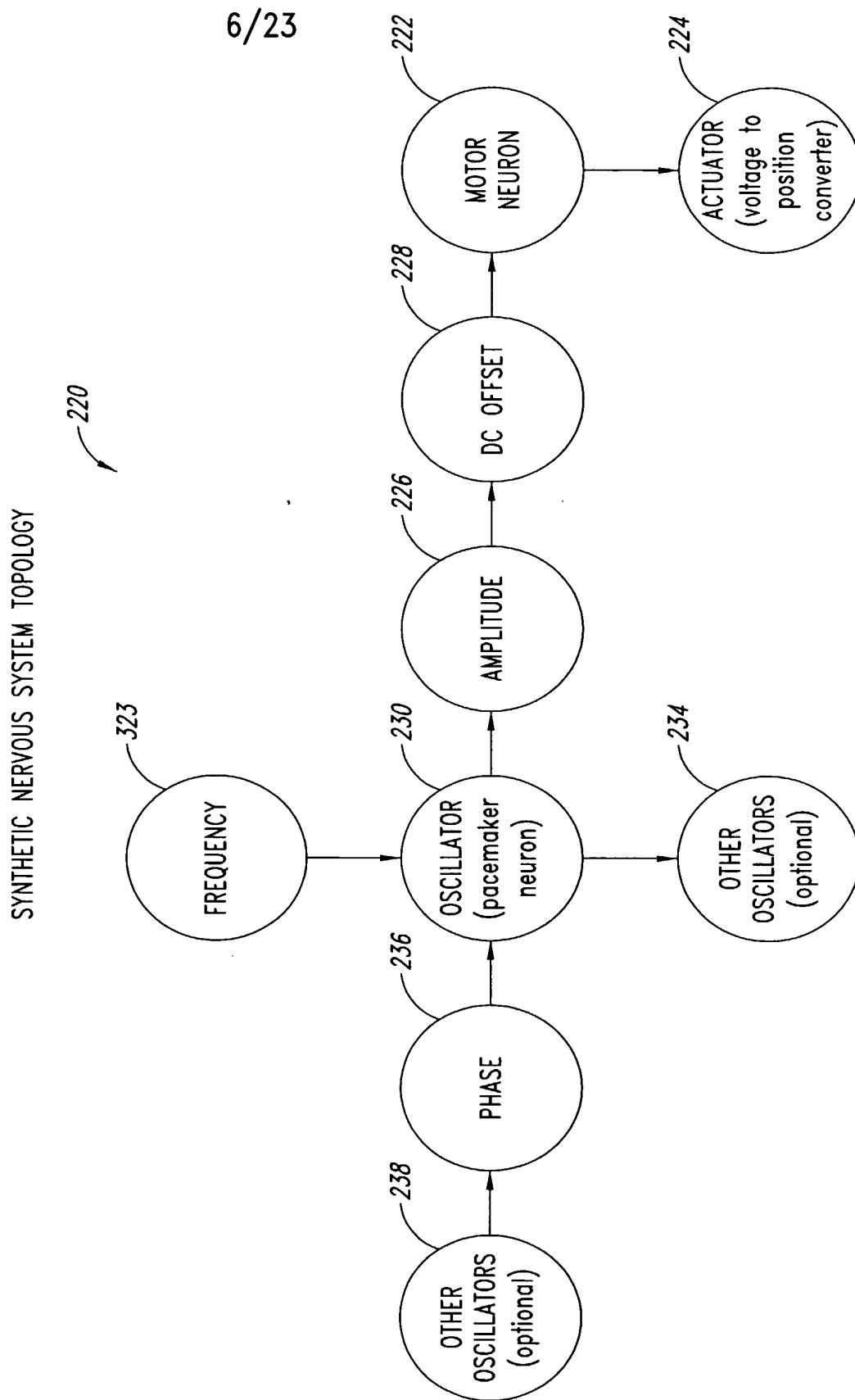
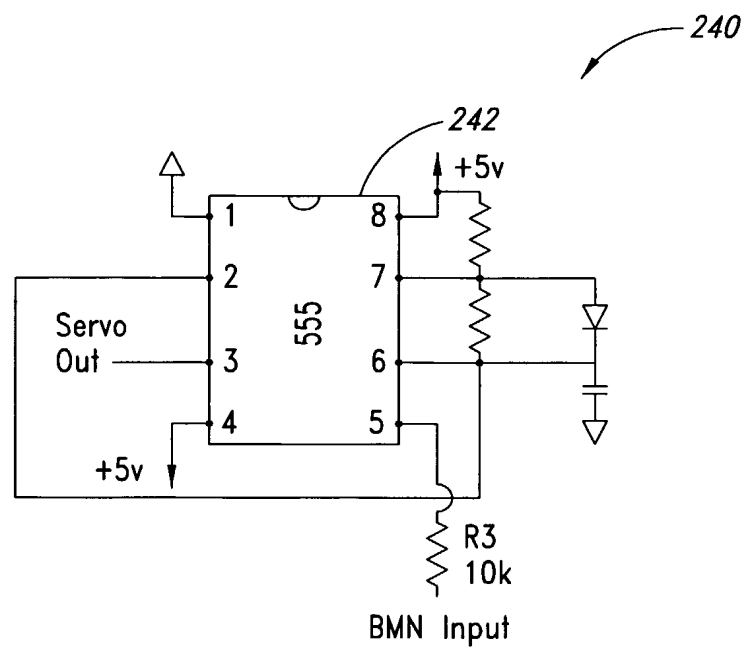


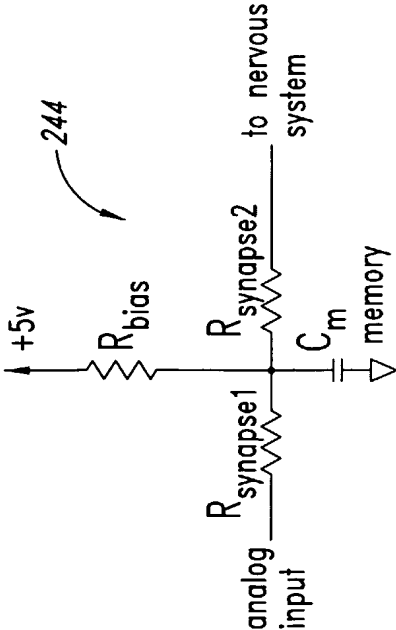
FIG. 8

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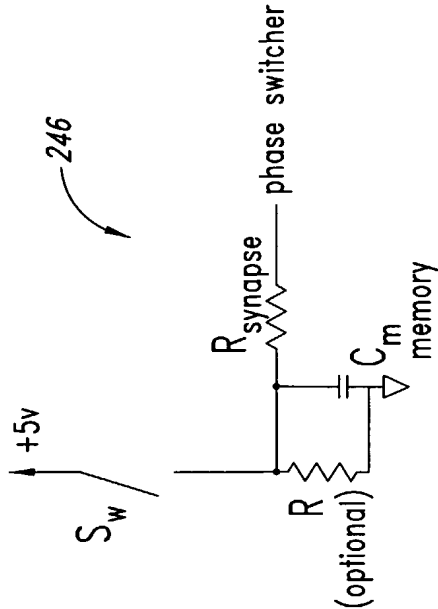
## 555 TIMER AS A MOTOR NEURON

*FIG. 9*

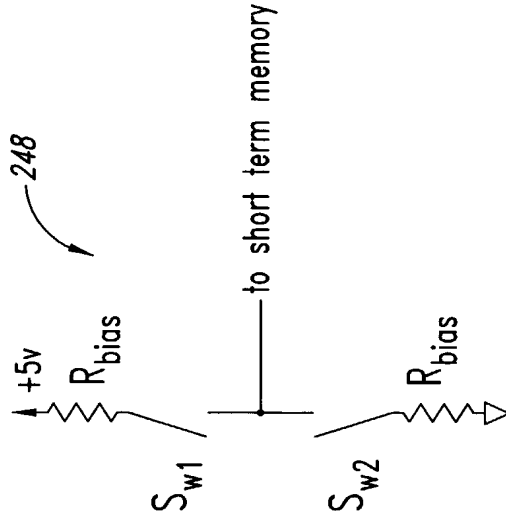
BASIC SHORT TERM MEMORY



SHORT TERM MEMORY FOR 2 SERVO WALKER



SIMPLE ANALOG INPUT TO SHORT TERM MEMORY





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NE567 TONE DECODER/PHASE-LOCKED LOOP AS A  
TIGHTLY COUPLED CENTRAL PATTERN GENERATOR

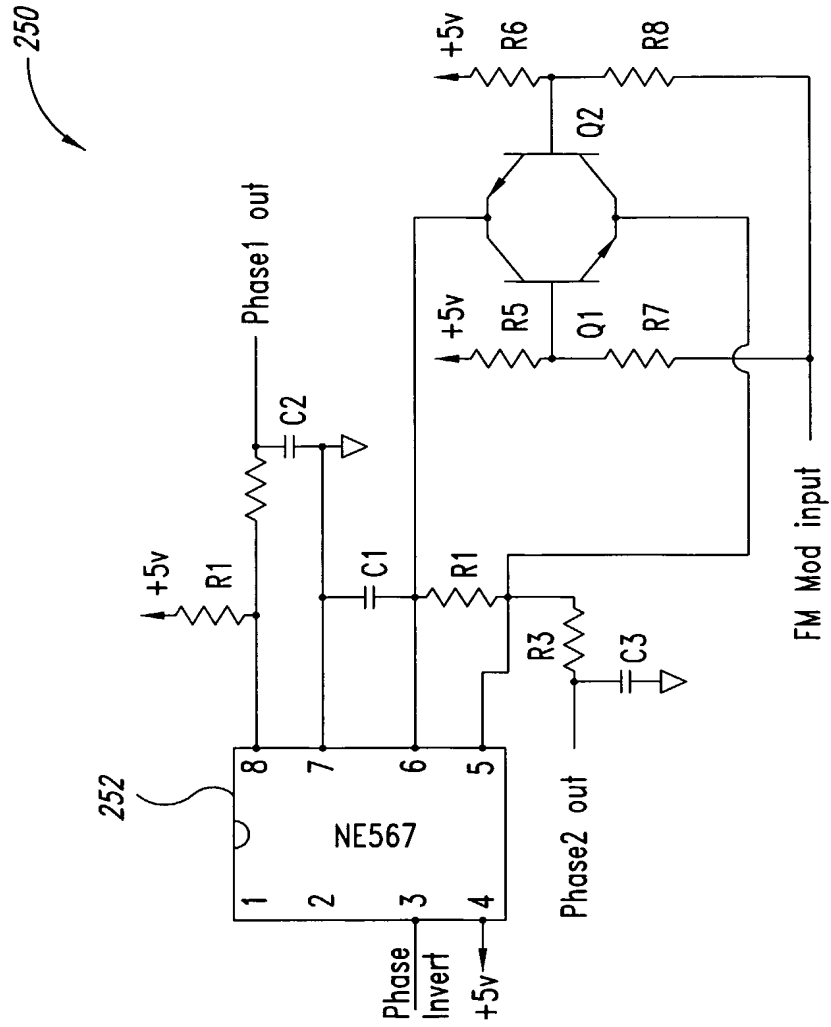
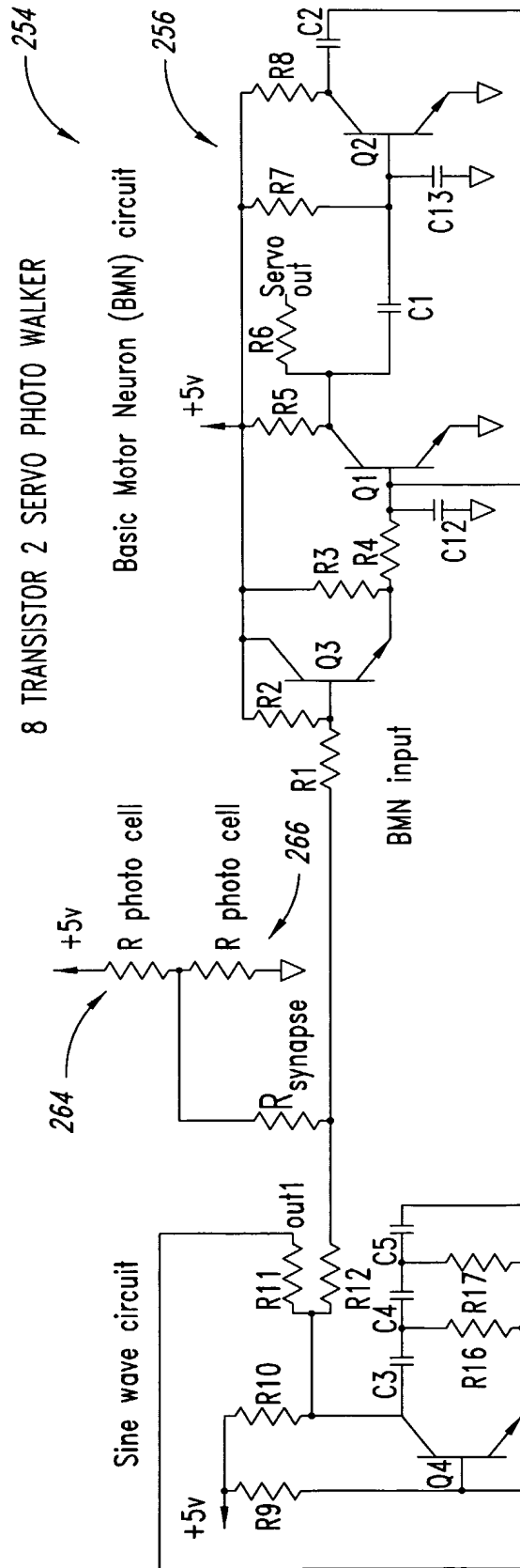


FIG. 11

8 TRANSISTOR 2 SERVO PHOTO WALKER



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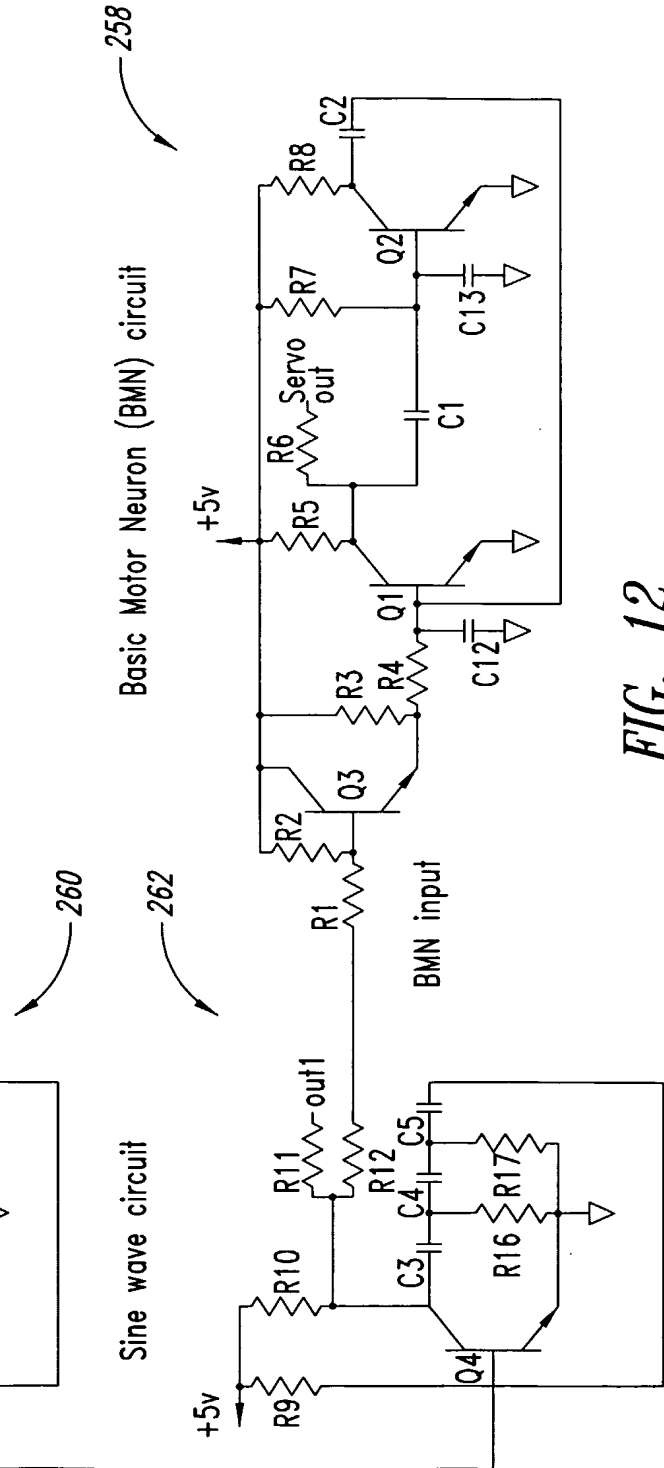


FIG. 12

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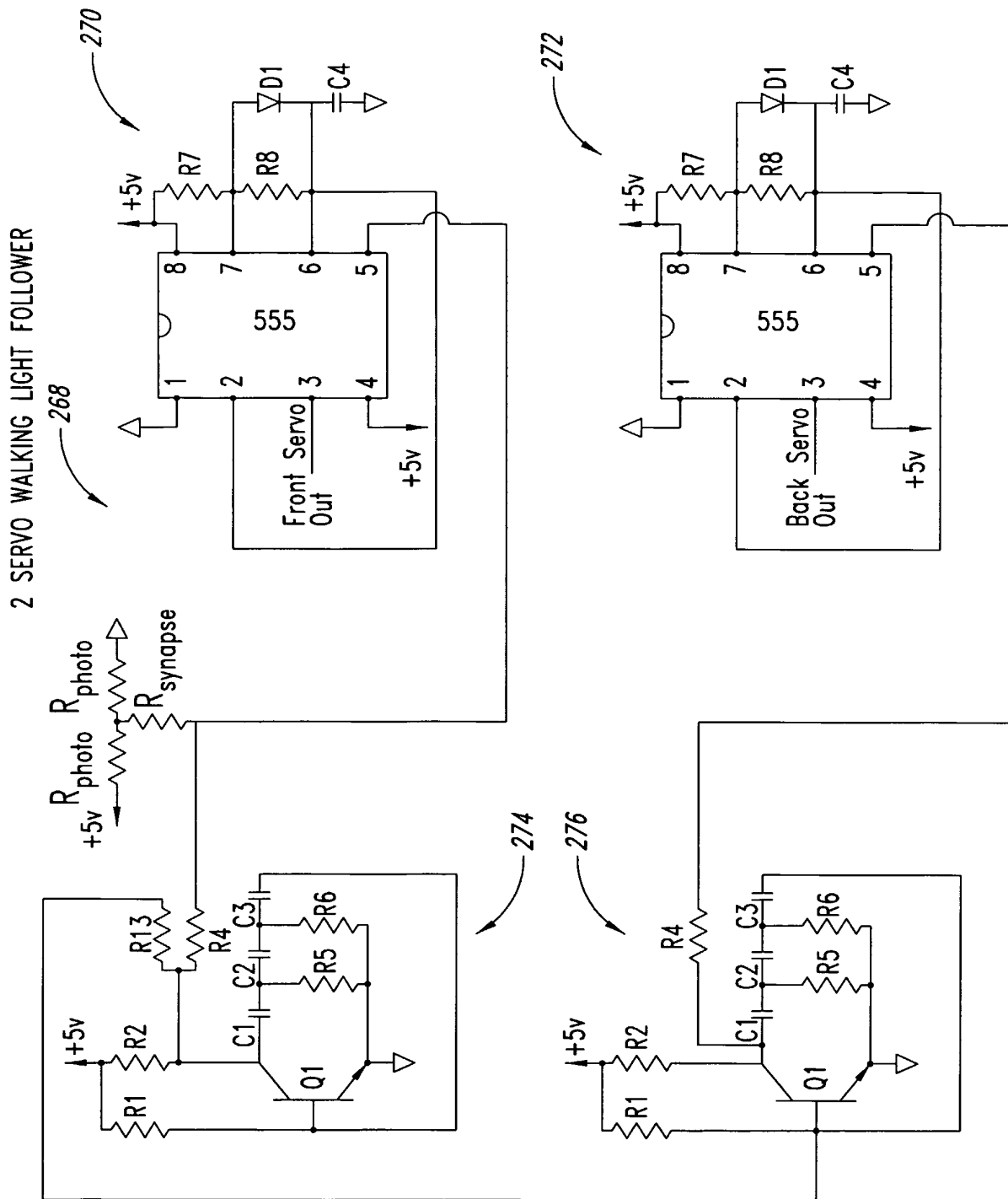
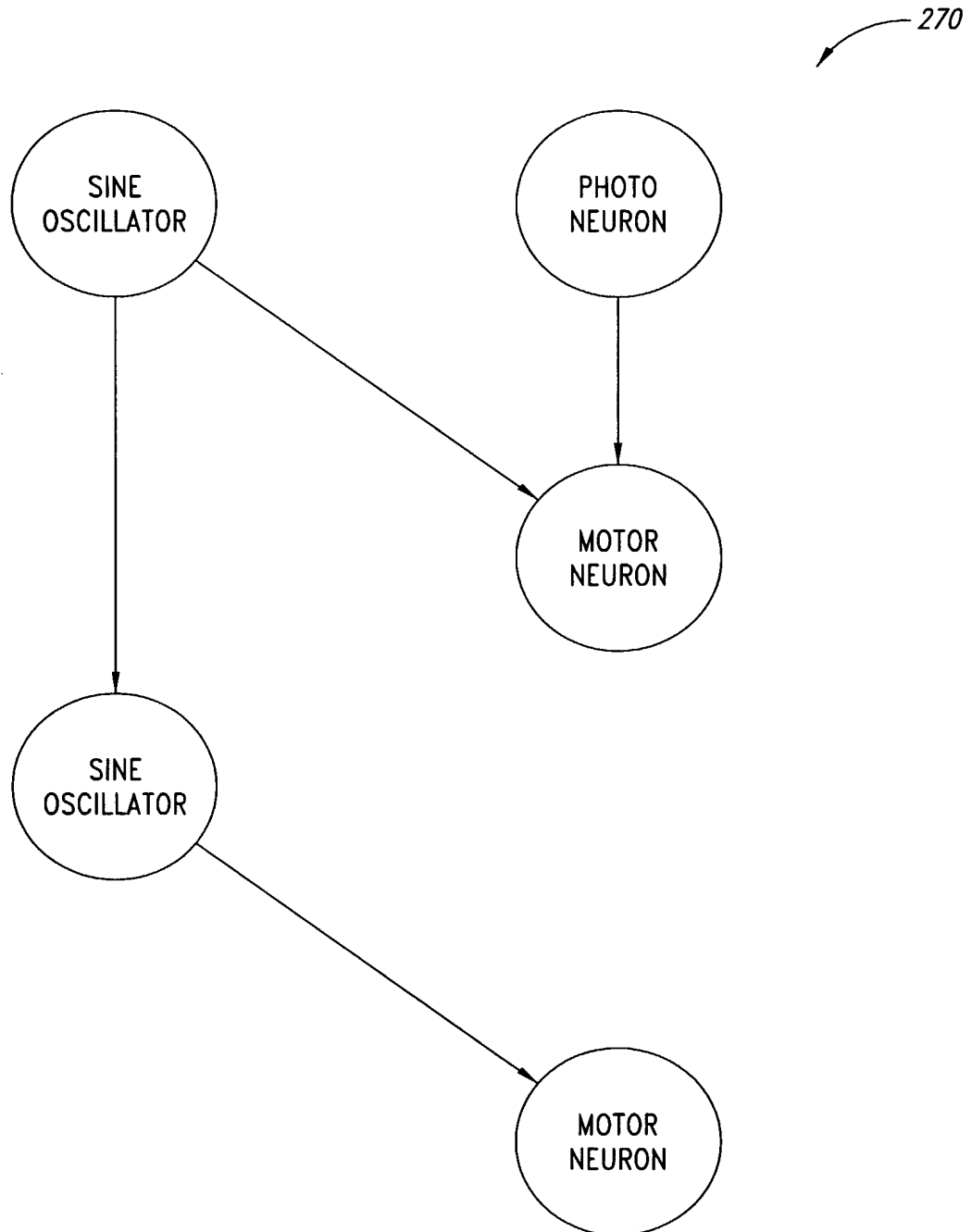


FIG. 13A

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*FIG. 13B*

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## PHASE SWITCH MATRIX WITH QUADPOD

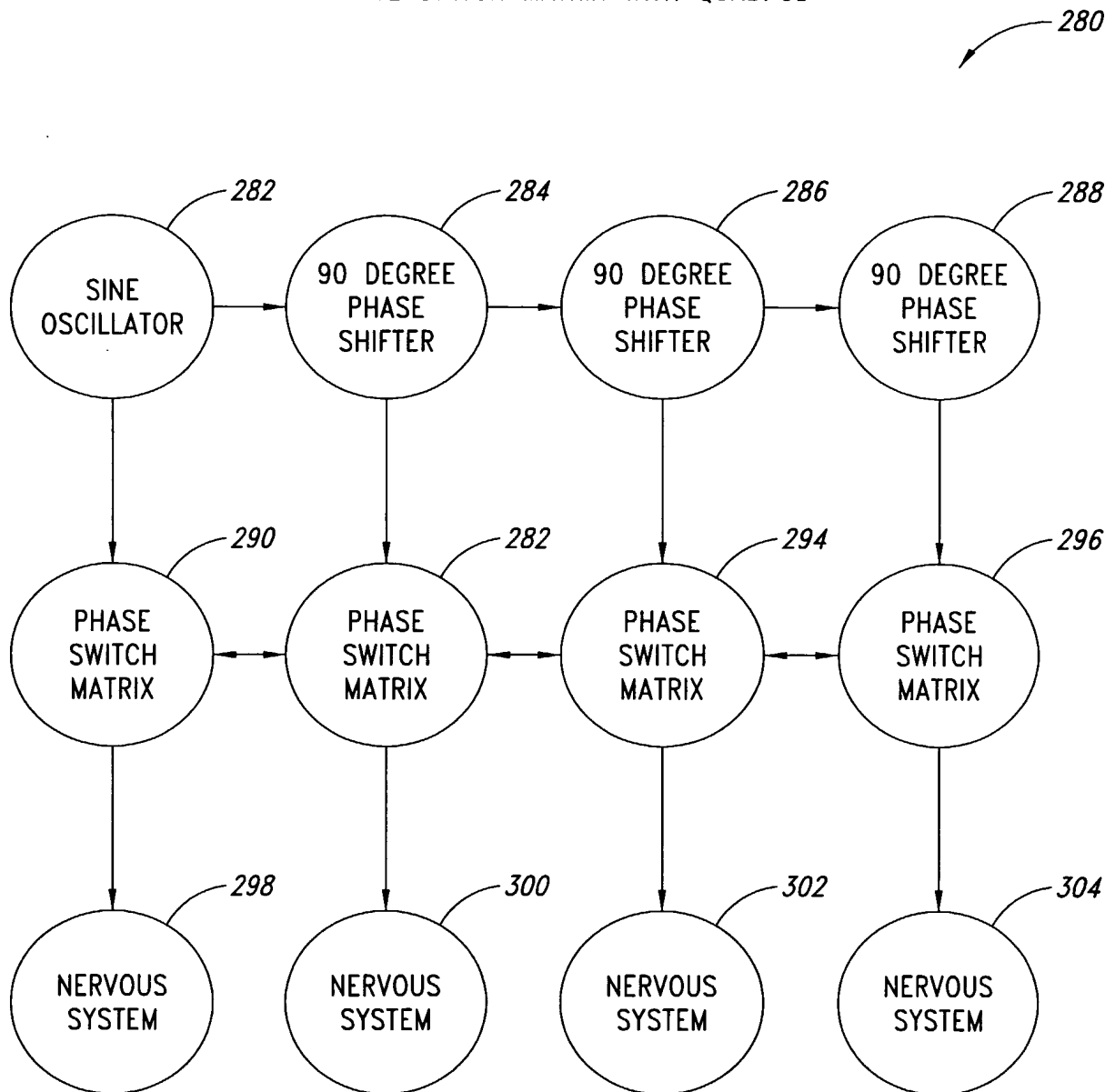
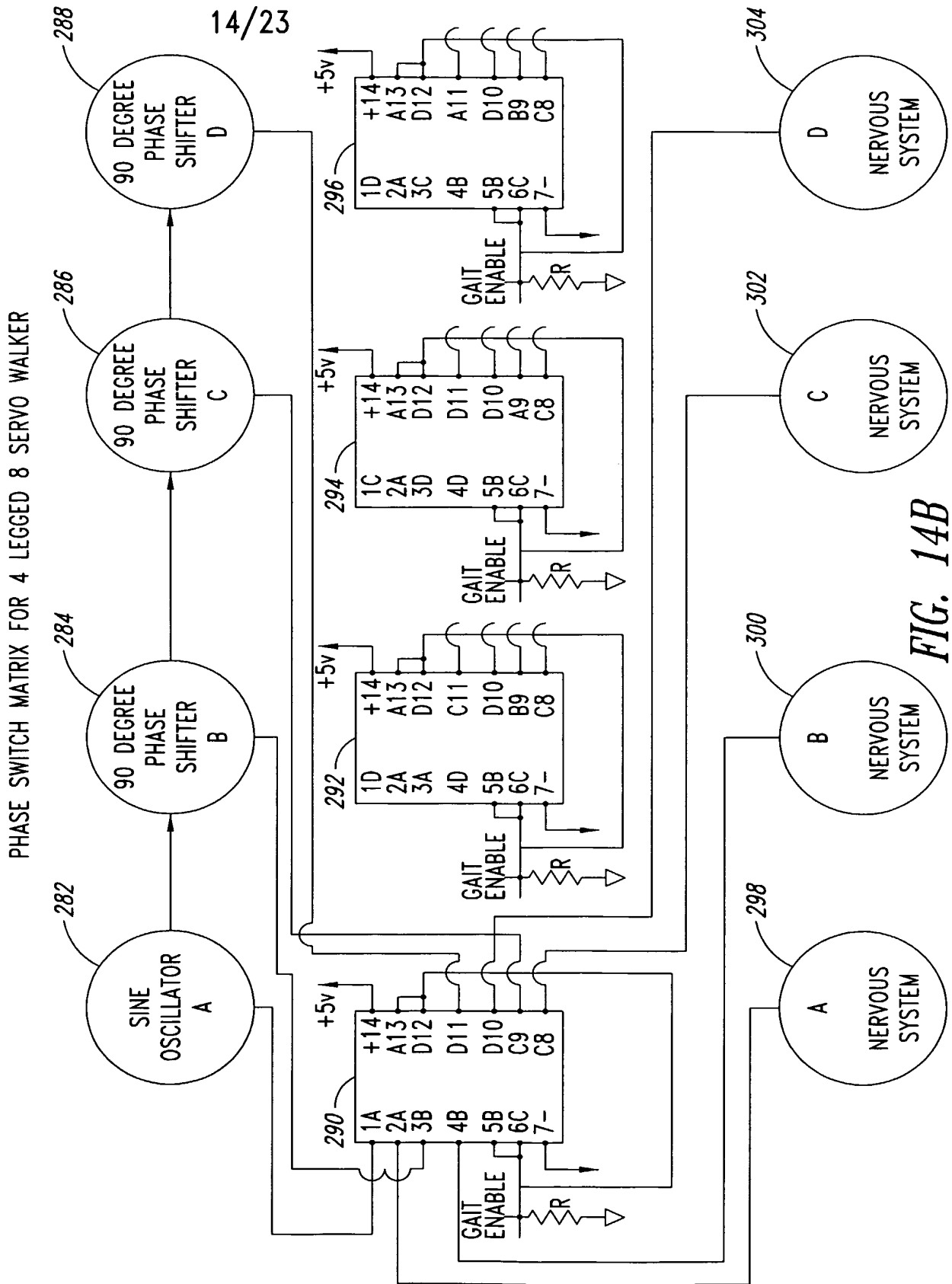
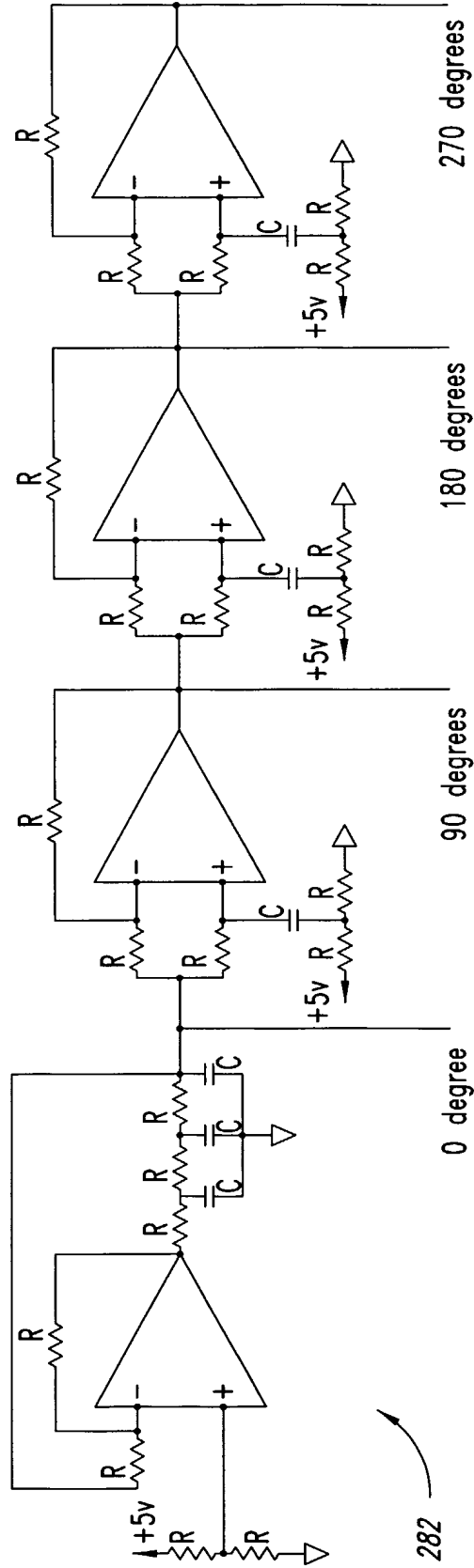


FIG. 14A



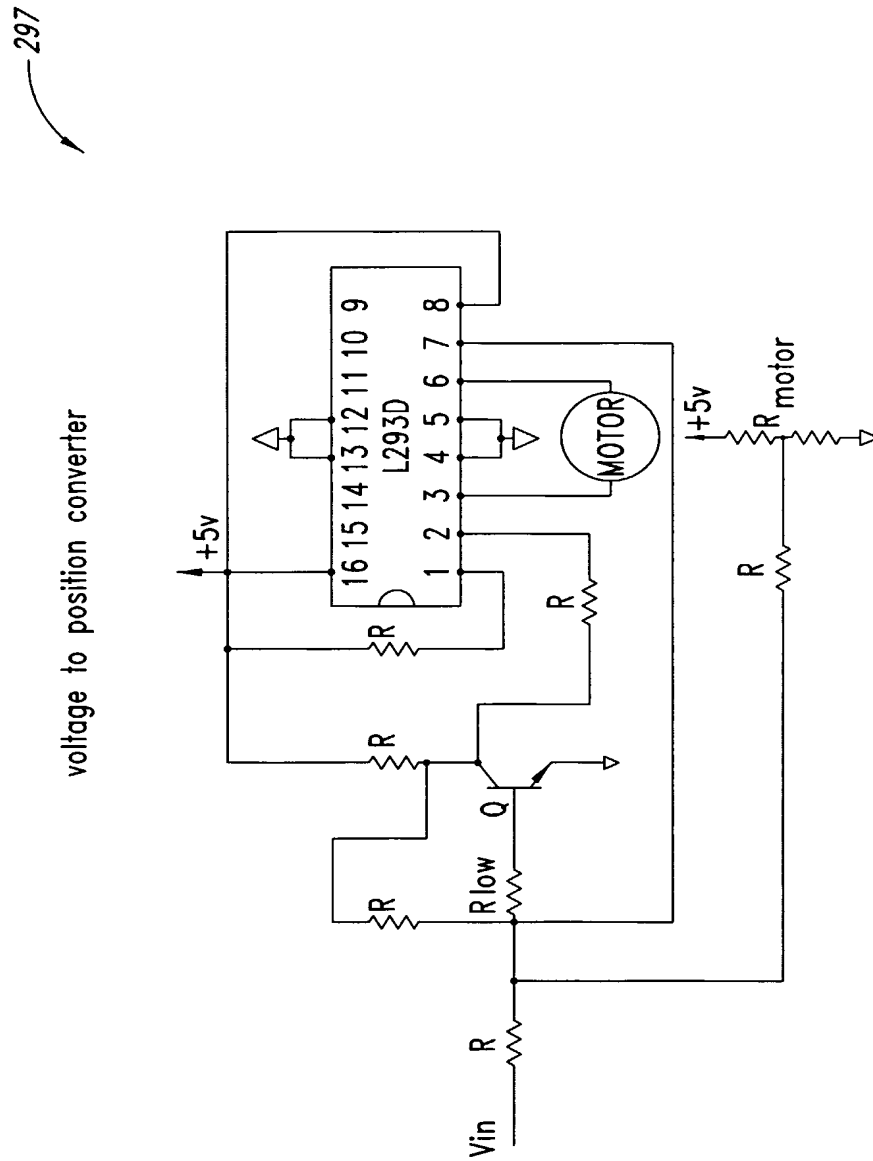
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QUAD TIGHTLY COUPLED CENTRAL PATTERN GENERATOR



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FIG. 14C



**FIG. 14D**



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LEARNING CONNECTIONIST SYNAPSE

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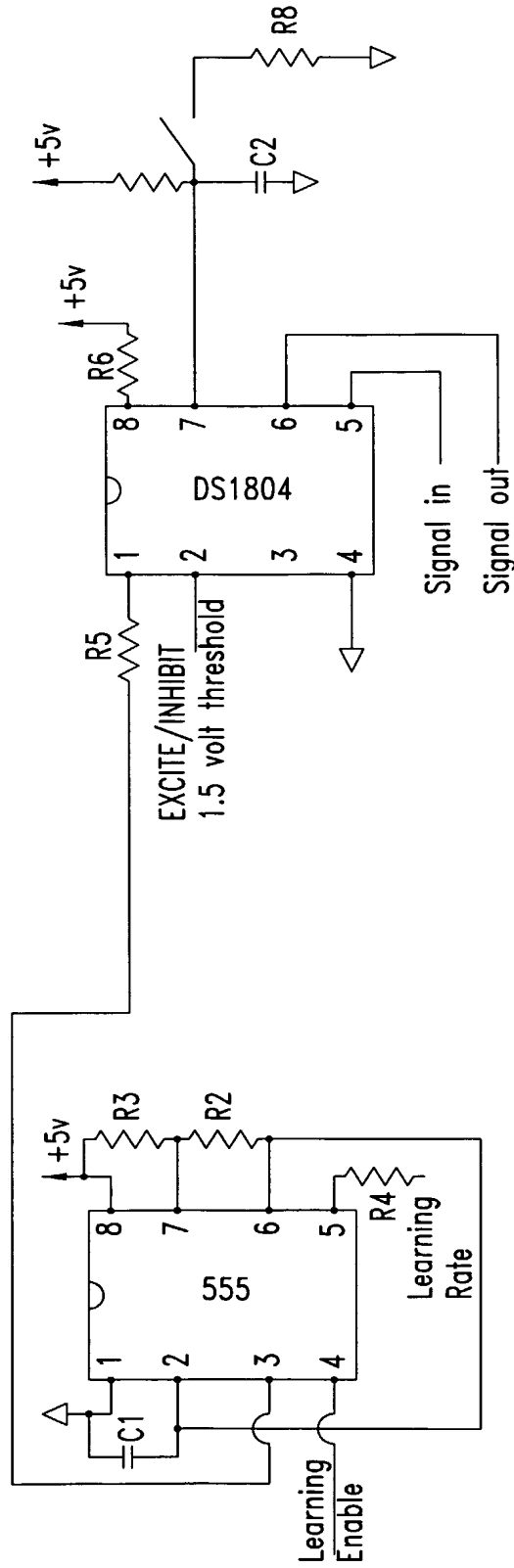


FIG. 15A

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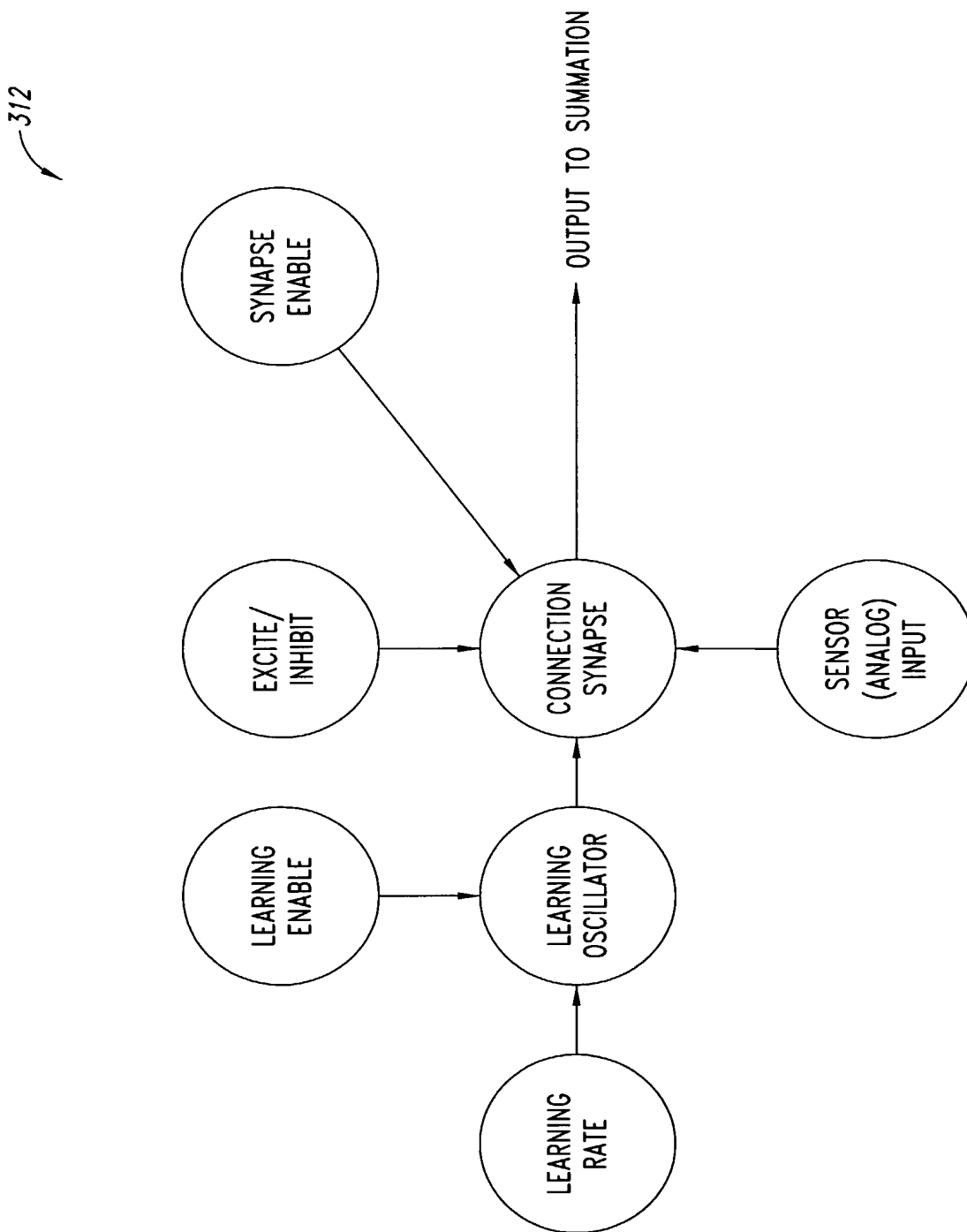


FIG. 15B

LEARNING CONNECTIONIST NEURON

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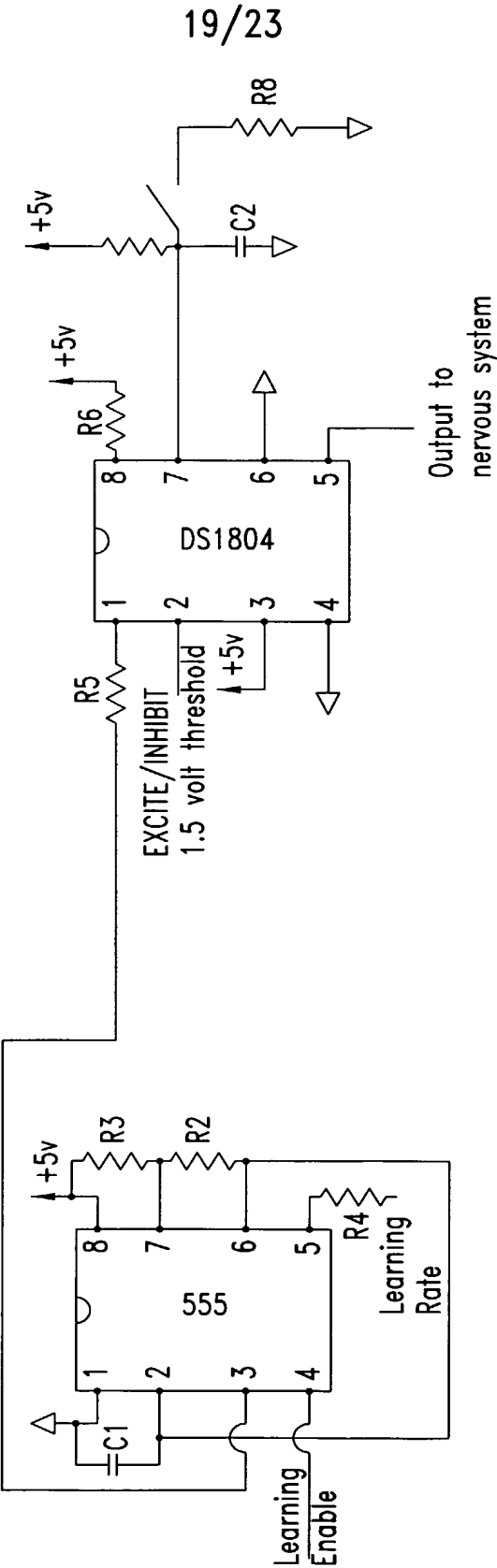


FIG. 16A

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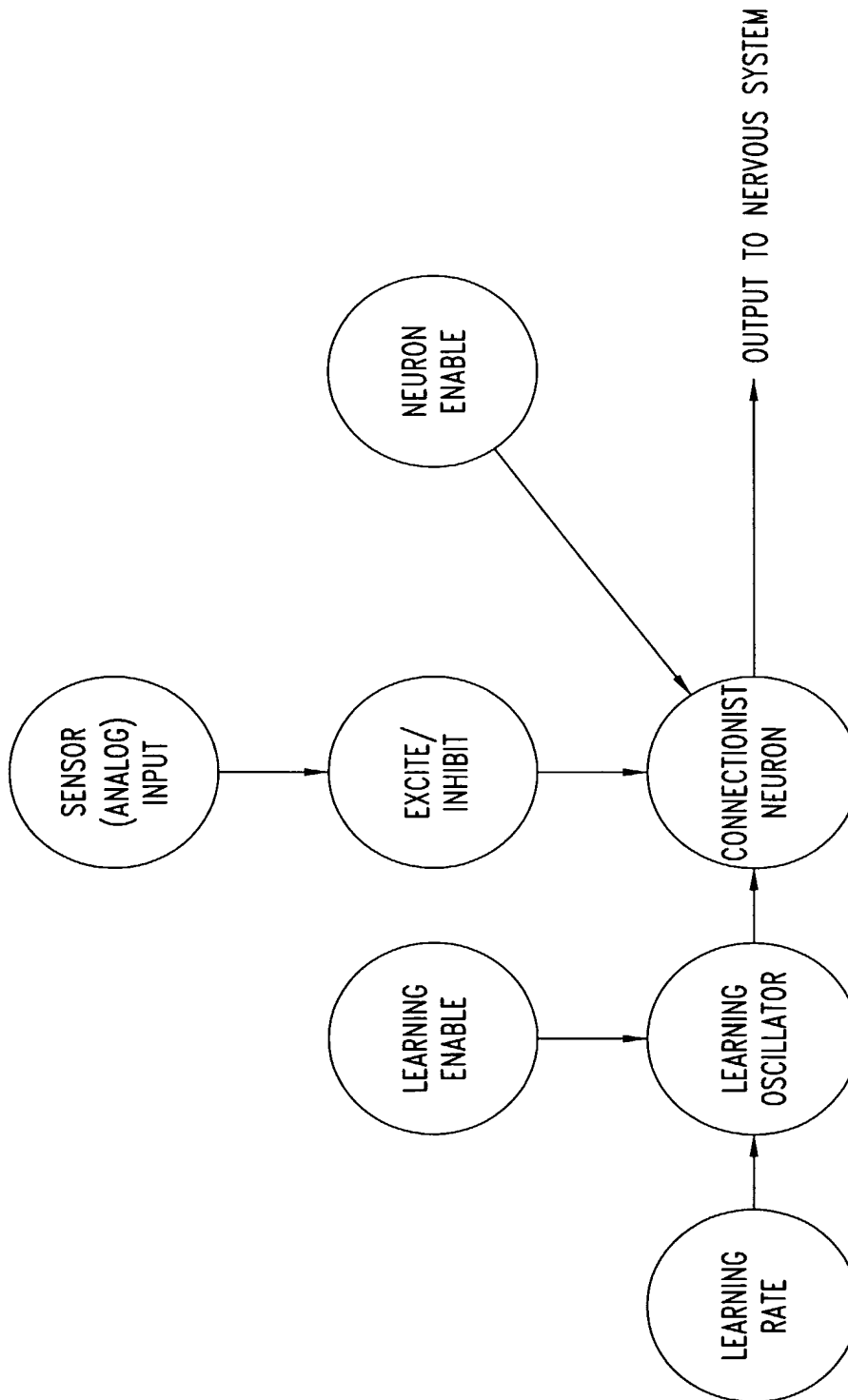
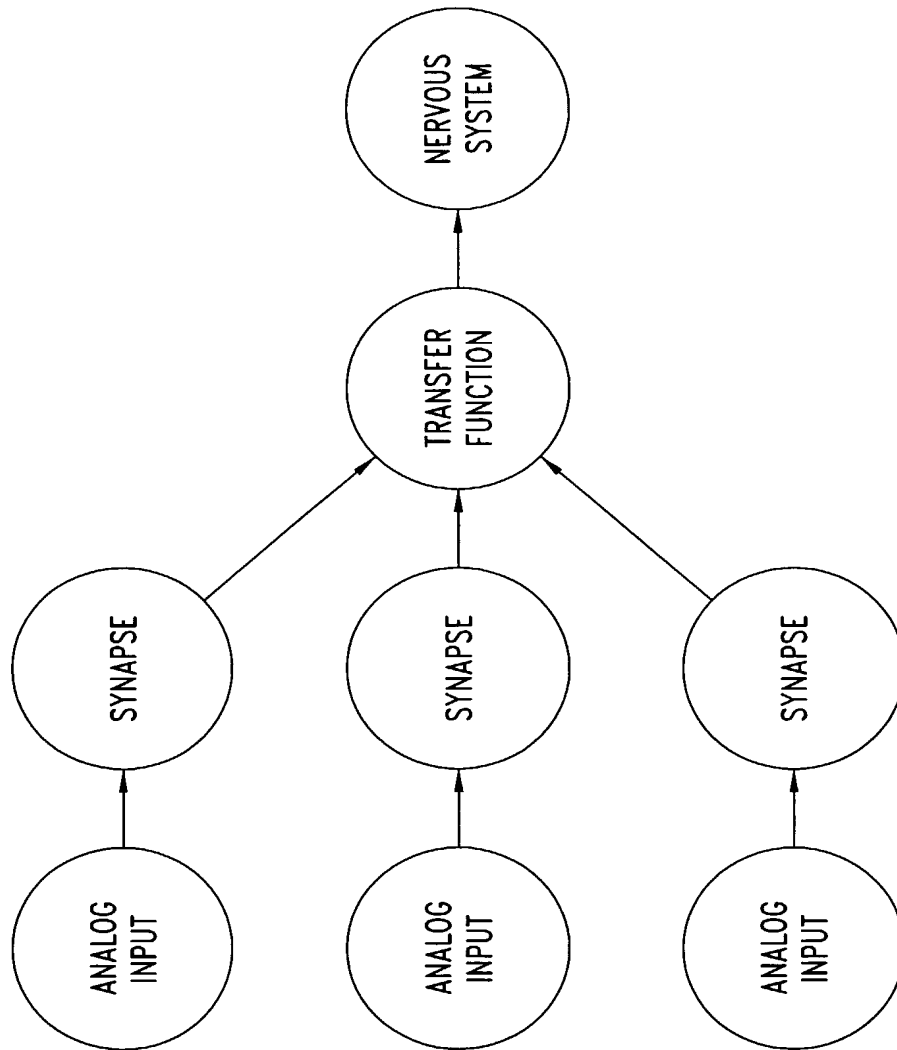


FIG. 16B

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EXAMPLE 3 INPUT SYNAPSE ARRAY

*FIG. 17*

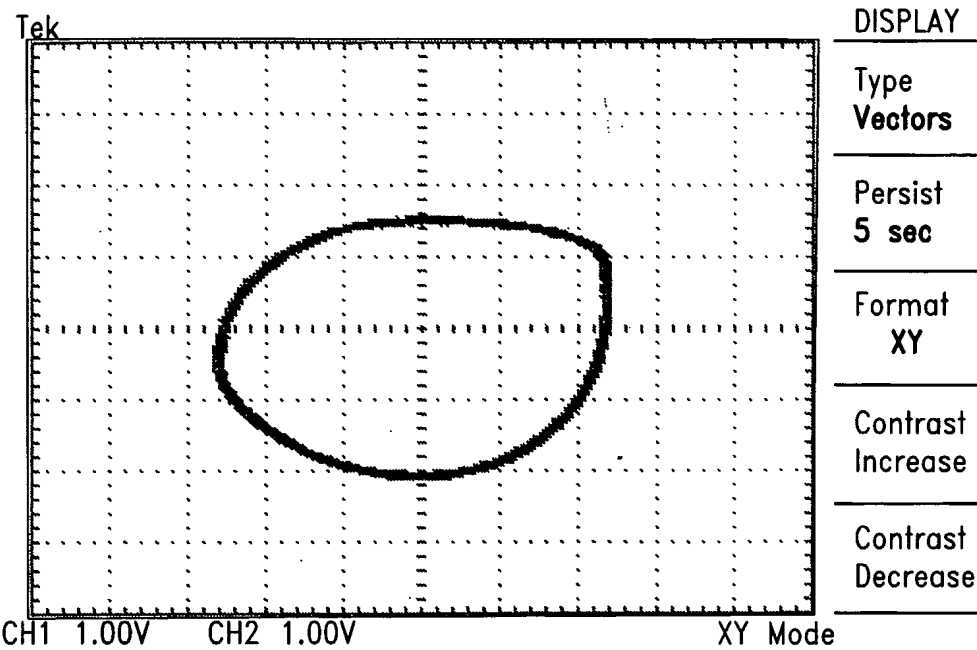


FIG. 18

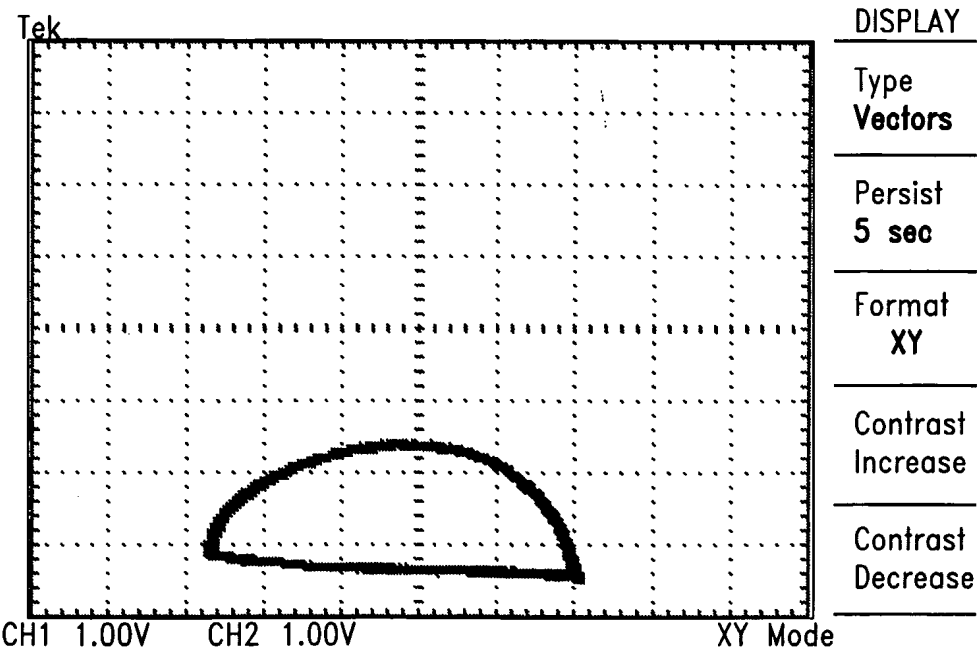


FIG. 19

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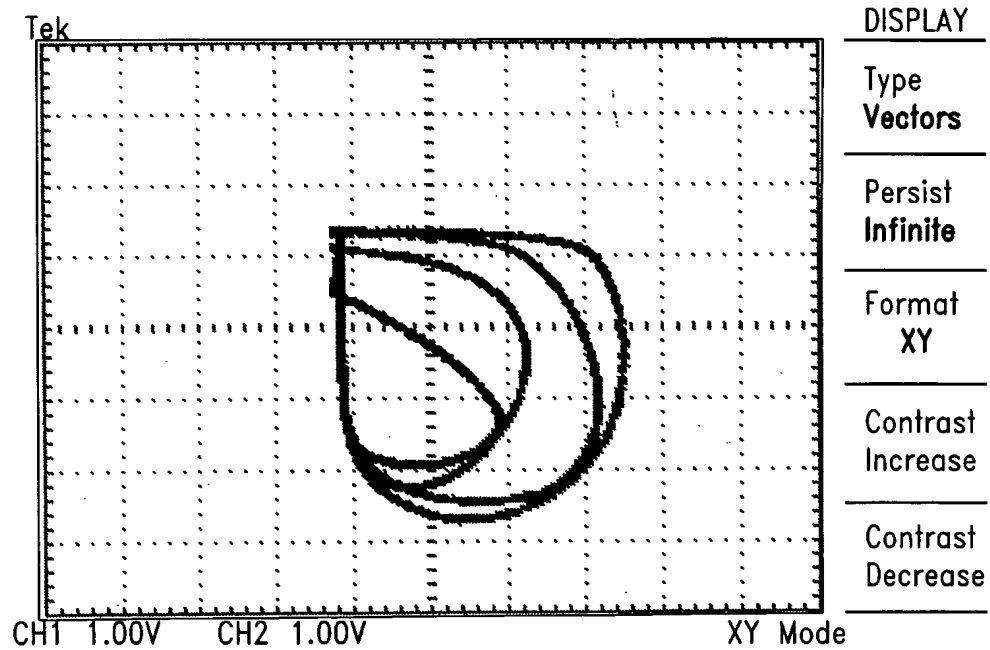


FIG. 20

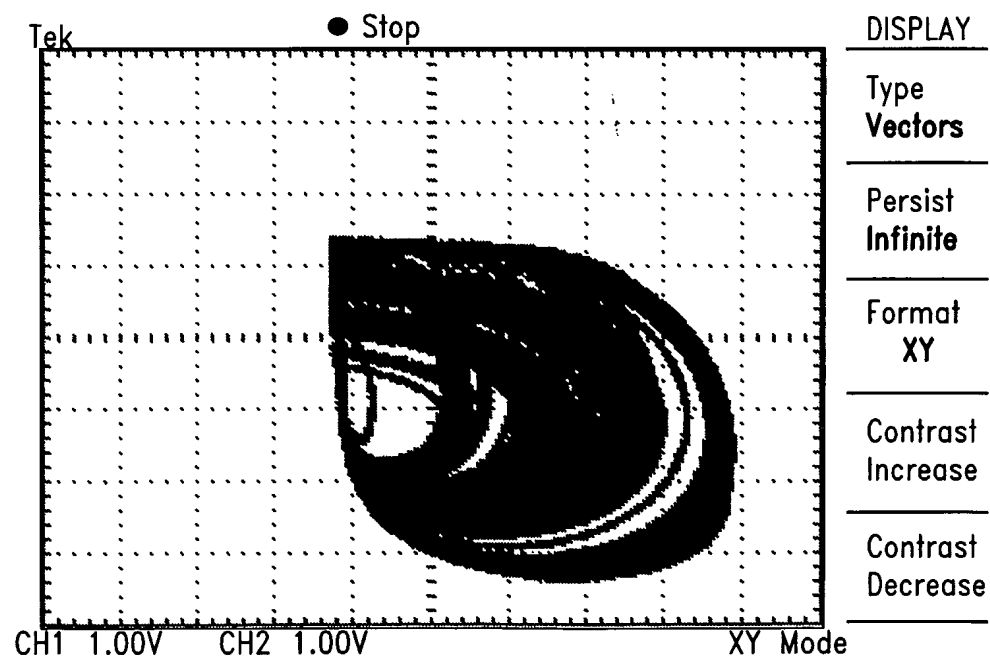


FIG. 21